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Design of Low power multipliers with Braun architecture using column bypassing multipliers

G.Balachandran*, N.Kandasamysuryaprakash, T.N.Devaprakash
Department of ECE, Jeppiaar Engineering College, Chennai, India
***Corresponding author: E-Mail: sg.bala81@gmail.com**

ABSTRACT

Signal processing computations like Fast Fourier Transforms involved stages of multiplication. Therefore it is necessary for a DSP system of modern world is in need of a low power multipliers for the reduction of the power which is dissipated. This paper mainly focuses on implementing the Low power Multiplier with Braun Architecture. The power reduction is mainly achieved by architecture optimization.

KEY WORDS: PP-Partial Products, CPA-Carry Propagation Addition.

1. INTRODUCTION

Binary multiplication consists of three basic steps: (i) Generation of partial products (PP). (ii) Reduction of partial products. (iii) Carry propagation addition (CPA). During the performance of multiplication area and power consumption is of major concern in VLSI system design. In a computing system multipliers usually occupies large area, long latency and they tend to consume large amount of power. This paper focuses in the reduction of the power consumed by the multiplier by using bypass multipliers. The main characteristics features of bypass multiplier is that the switching activity depends on the bit coefficient. If the bit coefficient is zero, the corresponding row and column will not be activated, as a result the power is reduced. If the multiplicand bit contains large number of 1s and 0s high power reduction is achieved.

Need for low power design: There is a need for low power design in modern electronics equipment in order to meet the better reliability. Usually low power design involves in two tasks to be computed they are Power estimation and analysis, power minimization. These tasks has to be followed some design hierarchy. It involves in behavioral, architectural, logic, circuit and physical levels. Recent survey stated that as the transistors increases (Moore's Law) the power consumptions also increases so it is necessary for a low power design in DSP systems.

Braun Architecture: A Braun multiplier is a m x n parallel multiplier. It is also known as carry save multiplier. It has m x n AND gates. The architecture of 4 x 4 Braun Multiplier array consists of (n-1) rows of carry save adders, in that each row has (n-1) full adders, the last row contains ripple adder for the propagation of carry.

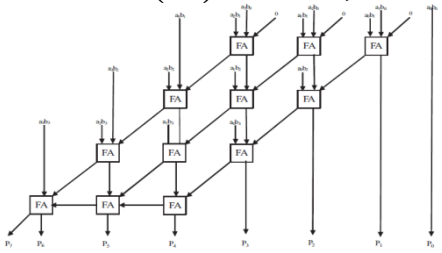


Figure.1. 4*4 Braun Multiplier

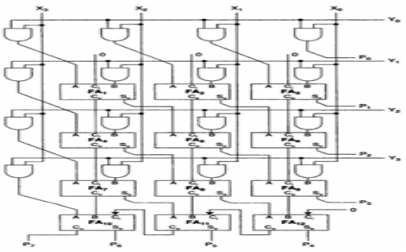


Figure.2. Internal Structure Of Braun Multiplier (Source :Ref (Moshnyaga, 1960)

Low Power Design Using Row Bypassing Multiplier: In case of adding the zero partial products produced by multiplication it leads to unnecessary transition of the signal. Therefore it is necessary to bypass the additions by disabling the adders. Row bypassing adder cell is given below in that if the j^{th} bit of b is 0, then the corresponding j^{th} row of the adder is not activated, the partial product is 0.

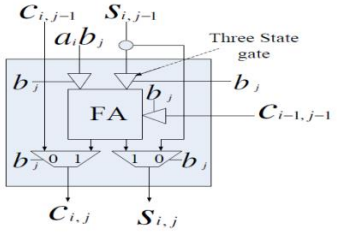


Figure.3. Row bypass adder cell (Source :Ref (Ohban, 2002)

The Row bypass adder cell consists of (n-1)×(n-1) full adders, 2×(n-1)×(n-1) multiplexers, and 3×(n-1)×(n-1) three state gates.If the cell encounters any of the zero partial product the adder cell disable the unwanted transitions and bypass the inputs to the outputs. The two multiplexers at the output stage involved transmitting input sum and carry bits of the previous addition to output. The tristate buffers are used to disable the unwanted transitions to the adders if they are bypassed. Its mainly involved in passing the input sum and carry bits downwards. By reducing the

switching activity of the logic circuit the power consumption will also be reduced. Thus the operation at j^{th} row is bypassed such that the output from the $(j-i)^{th}$ row is transformed to $(j+1)^{th}$ row, the multiplication output is not affected. The design has three trisate buffers and two 2 x1 multiplexers so that if any of the rightmost Full adders rows are bypassed, the additional circuits are added to get the multiplication results.

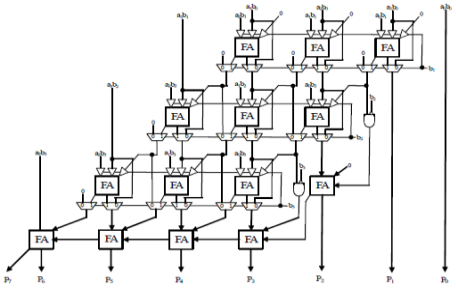


Figure.4. 4*4 Braun Multiplier With Row Bypassing(Source :Ref (Ohban, 2002)

multiplicand 1 1 1 a(i)

multiplier 1 0 1 b(J)

---

1 1 1 (J-1) th row

0 0 0 J th row

1 1 1 (J+1) th row

---

1 0 0 0 1 1

J-1 row directly bypassed to j+1 row

2. METHODS AND MATERIALS OF MULTIPLIER

The major drawback is that it needs some correction in the circuitry which in triangle. This makes the structure of the full adder more complex. So the drawback is replaced by the column bypassing multiplier which has a modified multiplier array design. It has only two trisate buffers and one 2 x 1 multiplexer.

Low power Design Using Column Bypassing Multiplier: In column by passing multiplier if the bit a_i in the multiplicand is 0 anywhere the entire $(i+1)^{th}$ column will be disabled. Thus the output carry must be given to the multiplexer to produce the correct output. The AND gate is used at the output of the last stage. The Column bypassing adder cell is shown. In that the unwanted transitions are bypassed, the sum input bits are passed downwards. When PPs are zero, Carry adder disables the unwanted transitions and bypass the input to the output.

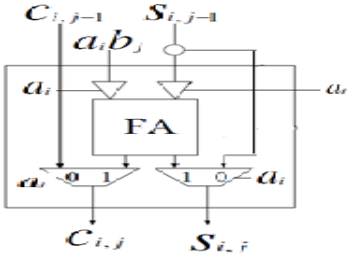


Figure.5. Column bypass adder cell (Source :Ref (Wen, 2005)

The modified full adder circuitry is simpler than that of row bypassing multiplexer. The multiplier desing consists of (n-1)*(n-1) full adders (n-1)*(n-1) multiplexers, and 2*(n-1)*(n-1) three state gates.

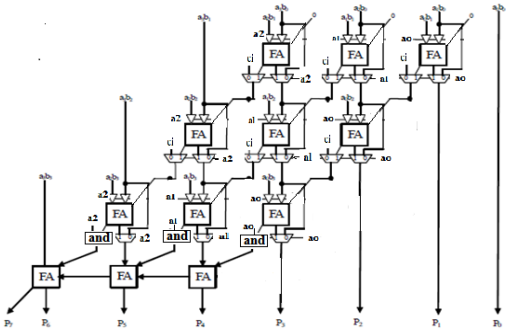
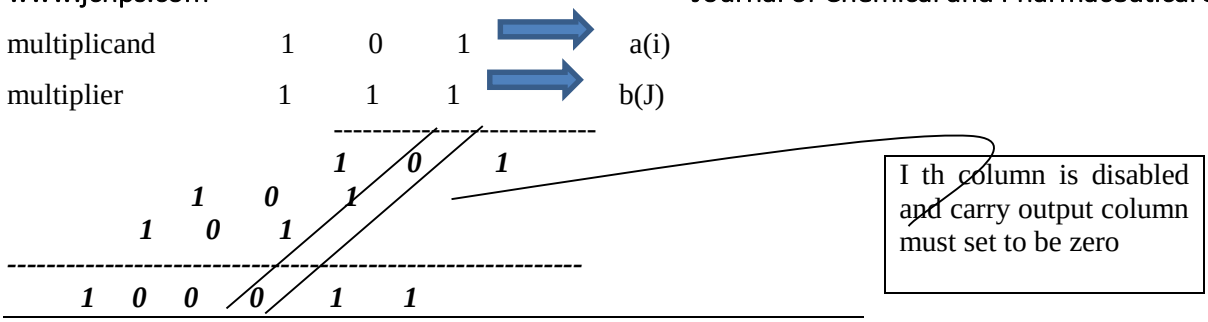


Figure.6. 4*4 braun multiplier with column bypassing (Source :Ref (Wen, 2005)



3. SIMULATIONS AND RESULTS

The tool used for the simulation and the analysis of the power is Xilinx software.

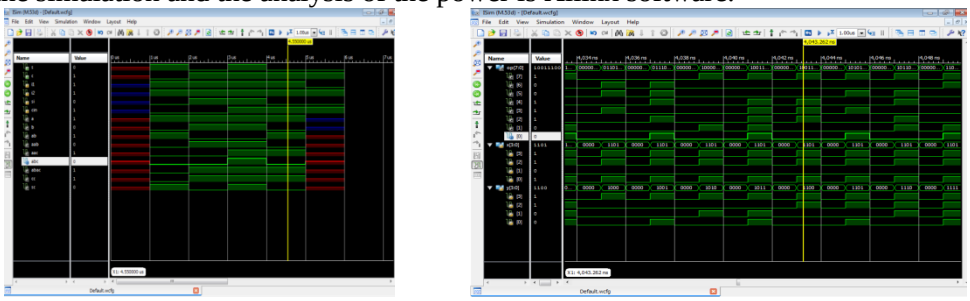


Figure.7. Outputof Row Bypass Multiplier

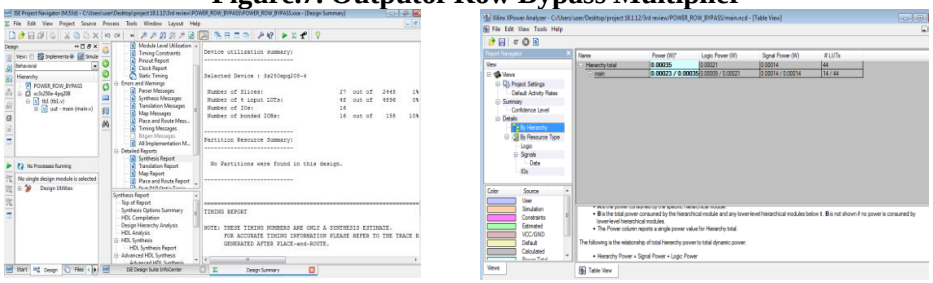


Figure.8. Power and area analysis of Row bypass multiplier

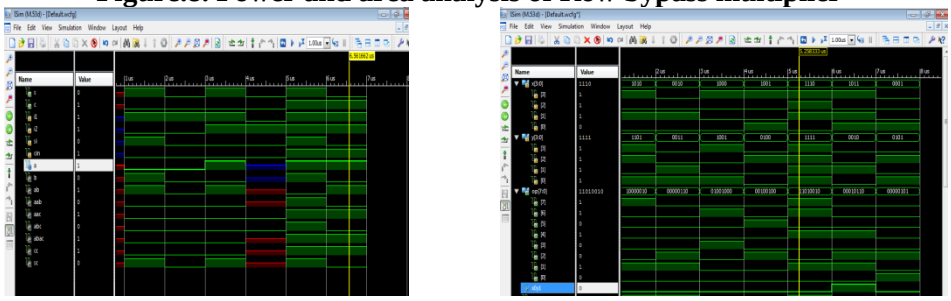


Figure.9. Output of column bypass multiplier

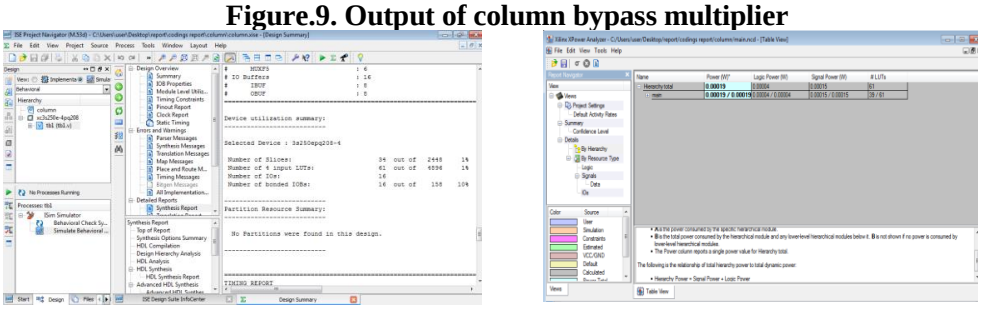


Figure.10. Power and area analysis of column bypass multiplier

Table.1.Comparion of Row and Column Bypass multiplier

Multiplier type	Array multiplier	Row bypass	Column bypass
Vendor	XILINX	XILINX	XILINX
Device and Family	Spartan 3E	Spartan 3E	Spartan 3E
Logic power	0.00136	0.00020	0.00004
Signal power	0.00053	0.00024	0.00015
Total power(w)	0.00189	0.00044	0.00019

Table.2. Comparison of column and row bypass multiplier

Multiplier Type	Array Multiplier	Row Bypass	Column Bypass
No. of Slices	19	27	33
LUT	35	48	61

4. CONCLUSION

We can design the Low power Multiplier by reducing the switching activity of the logic circuit without which their function is being changed. Thus from this one can say that adders are used for bypassing in a given situation. Thus column bypass multiplier has low power dissipation and it is suited for DSP applications. By using multipliers we can extend this to signal gating to multipliers such as partitionable multipliers and saturating multipliers.

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